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REMARKS

Claims 1-25 are pending in the present application, were examined, and were rejected. Applicant amends Claims 1, 2, 4, 6, 9, 10, 12, 15-17, 19 and 21-23 and reserves the right to prosecute the former claims in a divisional or continuation application. Applicant also adds Claims 26-30. Applicant respectfully requests reconsideration of pending Claims 1-30 and in view of at least the following remarks.

I. Claims Rejected Under 35 U.S.C. §102

The Patent Office rejects Claims 1, 2, 10, 16 and 22 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,742,788 to Priem et al. ("Priem1"). Applicant respectfully traverses this rejection.

Applicant respectfully asserts that the Examiner has failed to adequately set forth a *prima facie* rejection under 35 U.S.C. §102(b). "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik v. American Hoist & Derrick* ("Lindemann"), *730 F.2d 452, 1458 (Fed. Cir. 1994)*(emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. *Titanium Metals Corp. of American v. Banner* ("Banner Titanium"), *778 F.2d 775, 777 (Fed. Cir. 1985).*

In response to the Examiner's rejection of independent Claim 1, Applicant amends independent Claim 1 to include the following feature, which is neither nor suggested by either Priem1 or the references of record:

> a controller to copy identified data updated within the frame buffer to the second frame buffer and a display monitor when the identified data is needed to refresh the display monitor.

As indicated by the Examiner, Priem1 discloses a dual frame buffer system in FIG. 3 of Priem1, including a first frame buffer 43, a second frame buffer 44 and control circuits 41 and 42

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for copying data from the first frame buffer to the second frame buffer when data is changed in the first frame buffer and data is needed for refreshing the display monitor.

However, in contrast to the Examiner's contention and as clearly illustrated by careful review of FIG. 3, Priem1 provides:

> a single array of contiguous memory 42, which may be configured in various buffer arrangements in response to the software being run. The array 42, which may be configured into buffers, is constructed of VRAM and is two separate serial output terminals when providing data from a first portion (preferably half) of the array 42 and the other providing data from a second portion of the array 42 (col. 7, lines 50 -58).

Applicant submits that Priem1 teaches the use of a single buffer with dual output ports in contrast to first and second frame buffers, as required by Claim 1 of the present invention.

Furthermore, Claim 1, as amended, includes a first frame buffer into which updated data is written, as well as the second frame buffer which is used to store data used to refresh the display monitor. In contrast to the system described by Priem1, the controller copies identified updated data within the first frame buffer to the second frame buffer and the display monitor when the identified data is needed to refresh the display monitor.

In other words, data refresh is generally performed using the bandwidth of the second frame buffer. However, if data is updated within the first frame buffer following completion of a most recent refresh cycle, such data is scanned or updated to the display monitor during a refresh cycle. As a result, although the majority of the bandwidth for refresh is performed using the second frame buffer, occasion refresh of updated data within the first frame buffer is concurrently performed. Consequently, the first frame buffer may be utilized to perform other tasks.

In contrast, the system as taught by Priem1 may configure its array of VRAM 42 to support two frame buffers such that data may only be scanned from a designated frame buffer portion. As described at col. 11, lines 1-37, the system may operate in a mode DBMN in which it renders new data into an invisible frame buffer of the array from which data is never scanned to the display 48 in

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the manner described in co-pending patent applications first mentioned above (col. 11, lines 5-9). Furthermore, Priem1 also indicates:

> the fact that a particular portion of the array 42 is never scanned to the display is controlled by the multiplexor 45 on receipt of signals from the control circuits 40 and 41. (col. 11, lines 18–21.)

In other words, multiplexor 45 can only scan data from one of the designated portions of array 42; simultaneous scanning is prohibited. In contrast, Claim 1 requires a controller to copy identified updated data within the first frame buffer to the second frame buffer and a display monitor when the identified data is needed to refresh the display monitor. This is performed in conjunction with the second frame buffer which stores data used to refresh the display monitor. In other words, Claim 1 describes a system wherein data refresh is performed with the contents of a second frame buffer. However, in the event of updated data within a first frame buffer, the controller coordinates writing of the updated data to the display monitor in conjunction with the refresh of data to the display monitor using the data contained in the second frame buffer.

Applicant submits that the designation of a portion of the array 42, which is never scanned to the display, prohibits the Examiner from establishing a teaching or suggestion within Priem1 to the aforementioned controller. To wit, the case law is quite clear in requiring that anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention. *Id.*

Therefore, for at least the reasons described above, Applicant respectfully submits that the Examiner has failed to establish a *prima facie* rejection of Claim 1 over Priem1. Applicant submits that for at least the reasons described above, Claim 1 is patentable over Priem1 as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claim 1.

Regarding Claims 2-8, Claims 2-8 depend from Claim 1 and therefore include the patentable claim features of Claim 1. Accordingly, for at least the reasons described above, Claims

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2-8 are patentable over the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claim 2.

II. Claims Rejected Under 35 U.S.C. §103

The Patent Office rejects Claims 3 and 11 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,742,788 to Priem et al. ("Priem1") as applied to Claim 1 and further in view of U.S. Patent No. 5,724,608 to Tohara ("Tohara") and further in view of U.S. Patent No. 5,543,824 to Priem et al. ("Priem2"). Applicant respectfully traverses this rejection.

Regarding Claim 3, Claim 3 depends from independent Claim 1 and therefore includes the patentable claim features as described above with reference to Claim 1. Applicant submits that the teachings of both Tohara as well as Priem2 do not rectify the deficiencies attributed to Priem1's failure to teach or suggest the controller for copying updated data to both the second frame buffer and the display memory. Therefore, for at least the reasons described above, Claim 3 is patentable over the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 3.

Regarding Claim 11, Applicant submits that Claim 11 is dependent from Claim 9 and therefore includes the patentable claim features of Claim 9, which is amended, to include a controller as described above with reference to Claim 1. As indicated above, the Examiner's citing of Tohara as well as Priem2 do not rectify the deficiencies attributed to Priem1 in order to render Claim 11 obvious over Priem1 in view of Tohara and further in view of Priem2. Consequently, Applicant submits that the Examiner fails to establish a *prima facie* rejection of Claim 11 under 35 U.S.C. §103(a). Therefore, Applicant respectfully requests the Examiner reconsider and withdraw the §103(a) rejection of Claim 11.

The Patent Office rejects Claims 4-6, 12-15, 17-19, 21, 23-24 and 25 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,742,788 to Priem et al. ("Priem1") as applied to Claim 1 and further in view of U.S. Patent No. 5,724,608 to Tohara ("Tohara") and further in view of U.S. Patent No. 5,543,824 to Priem et al. ("Priem2") as applied to Claim 3 and

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further in view of U.S. Patent No. 5,757,364 to Ozawa et al. ("Ozawa"). Applicant respectfully traverses this rejection.

Regarding Claims 4-6, Claims 4-6 depend from, and therefore include, the patentable claim features of Claim 1 as described above. Furthermore, the Examiner's citing of the Tohara reference, Priem2 reference, as well as the Ozawa reference, fails to rectify the deficiencies attributed to Priem1 for its failure to describe a controller which enables copying of updated data to both the display monitor and second frame buffer when required to refresh the display monitor. Claims 4-6 describe detectors and decoders which enable the controller to concurrently refresh the display monitor from data contained in the secondary frame buffer as well as any updated data detected within the first frame buffer.

As indicated above, Priem1, as well as Priem2, strictly prohibit the simultaneous scanning of data from both frame buffers to the display. This is directly in contrast to the controller as described with reference to Claim 1, which enables such simultaneous scanning.

Accordingly, for at least the reasons described above, Applicant respectfully submits that Claims 4-6 are patentable over the references of record. Consequently, the Examiner cannot establish a *prima facie* rejection of Claims 4-6 over Priem1 in view of Tohara and further in view of Priem2, as all as Ozawa. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 4-6.

Regarding Claims 12-14, Claims 12-14 include features of the detectors and decoders which enable the controller of amended Claim 9 to concurrently refresh a display monitor using data contained within a secondary frame buffer, as well as updated data contained within a primary frame buffer. This feature is directly in contrast and taught away from by both Priem1 and Priem2 based on the aforementioned prohibition of the Priem1 and Priem2 references against simultaneous scanning of data from both the frame buffers to a display.

Accordingly, Applicant submits that the specific prohibition against simultaneous copying from frame buffers prohibits the Examiner from establishing a *prima facie* rejection of Claims 12-

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14. Consequently, Applicant respectfully requests the Examiner reconsider and withdraw the §103(a) rejection of Claims 12–14.

Regarding Claim 15, Claim 15 includes the following feature, which is neither taught nor suggested by the references of record:

> coordinating refreshing of the display monitor and copying identified data from the first frame buffer memory to a second frame buffer memory and a display monitor when the data is needed to refresh the display monitor.

As indicated above, this feature is specifically taught away from in Priem1 by Priem1's prohibition against simultaneous copying or scanning of data from both frame buffers. In other words, data contained within the second frame buffer is refreshed to a display monitor while any detected updated data is refreshed to the display monitor and simultaneously copied to the second memory buffer. Following the current refresh cycle, the updated data is contained within the second memory buffer such that during a subsequent refresh cycle, the first frame buffer memory may be free to be used for other tasks while the refreshing of the display monitor is performed using the contents of the second frame buffer memory.

Accordingly, based on the specific prohibit against dual frame buffer scanning, Applicant submits that the Examiner cannot establish a *prima facie* rejection of independent Claim 15 over either Priem1 in view of Tohara and further in view of Priem2 as well as Ozawa. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 15.

Regarding Claims 17-19, Claims 17-19 depend from Claim 15 and therefore include the patentable claim features of Claim 15 as described above. Accordingly, for at least the reasons described above, Claims 17-19 are patentable over the references of record. Consequently, Applicant respectfully requests the Examiner reconsider and withdraw the §103(a) rejection of Claims 17-19.

Regarding Claim 21, Claim 21 is amended to include analogous features to Claim 15 as described above in the form of a computer program product. Accordingly, for at least the reasons

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described above with reference to Claim 15, Applicant respectfully submits that the Examiner cannot establish a *prima facie* rejection of Clam 21 over the references of record. Consequently, Applicant respectfully requests the Examiner reconsider and withdraw the §103(a) rejection of Claim 21.

Regarding Claims 23-25, Claims 23-25 depend from Claim 1 and therefore include the patentable claim features of Claim 1 as described above. Consequently, Applicant respectfully submits that Claims 23-25 are patentable over the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 23–25.

The Patent Office rejects Claims 7-9 and 20 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,742,788 to Priem et al. ("Priem1") as applied to Claim 1 and further in view of U.S. Patent No. 5,790,138 to Hsu ("Hsu"). Applicant respectfully traverses this rejection.

Regarding Claims 7 and 8, Claim 8 depends from Claim 7, which includes a further claim feature of the first frame buffer as part of a unified memory architecture. In the Examiner's rejection, the Examiner proposes to modify Priem1 in view of Hsu, which the Examiner believes describes a first frame buffer as part of a unified memory architecture. However, after careful review of Priem1, Applicant respectfully submits that Priem1 teaches away from providing a first memory buffer as part of a unified memory architecture.

This proposition is based on the fact that Priem1 teaches a single frame buffer, which may be configured as a pair of frame buffers. However, as described within Priem1, frame buffer 42 is nothing more than a single array of contiguous memory 42, which may be configured in various buffer arrangements in response to the software being run. As a result, modification of Priem1 to provide a first frame buffer within a unified memory architecture would require either the inclusion of an additional frame buffer or the subdivision of the frame buffer 42, as depicted in Priem1.

According to the Examiner, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Priem1 with the feature frame buffer as part of the unified memory architecture because it provides for a lower system cost. However, the Examiner,

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as required by MPEP §2142, cannot show a suggestion or motivation to combine reference teachings unless there is a reasonable expectation of success in modifying the reference teachings. The Examiner has failed to address how an additional frame buffer, incorporated into a unified memory architecture, would function in conjunction with the frame buffer 42, as described with reference to FIG. 3. Furthermore, the Examiner has failed to address how the frame buffer 42 of Priem1 could be subdivided such that a portion of the frame buffer is designated within the unified memory architecture.

Consequently, Applicant respectfully submits that the Examiner cannot establish a *prima facie* rejection of Claim 7 since there is no teachings or suggestions to modify Priem1 in view of Hsu in violation of MPEP §2142. Accordingly, for at least the reasons described above, Applicant respectfully submits that Claim 7 is patentable over the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 7.

Regarding Claim 8, Claim 8 is dependent from Claim 7 and therefore includes the patentable claim features of Claim 7, as described above. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 8.

Regarding Claim 9, Claim 9 is amended to include a controller feature as described above with reference to Claim 1. As indicated, this controller feature enables an analogous simultaneous buffer refresh from the first and second frame buffer memories in violation of the stated prohibition of Priem1 from prohibiting simultaneous scanning of data from both portions of the buffer array.

Furthermore, Claim 9 includes the primary frame buffer as part of a unified memory architecture. As described with reference to Claim 7, the Examiner fails to address the issues of a reasonable expectation of success in modifying Priem1 to include the frame buffer within a unified memory architecture, as such modification would most likely require the subdivision of the frame buffer array 42 as required by Priem1.

Accordingly, for at least the reasons described above, Applicant respectfully submits that the Examiner cannot establish a §103(a) rejection of Claim 9 since the cited references by the Examiner do not teach each and every element of Claim 9 and the Examiner fails to establish a reasonable

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expectation of success in modifying the reference teachings. Consequently, for at least the reasons described above, Claim 9, as amended, is patentable over the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 9.

Regarding new Claims 26-31, new Claims 26-31 include the patentable claim features as described above and are therefore patentable over the references of record.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: June 6, 2003

By: _____
Joseph Lutz, Reg. No. 43,765

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Commissioner for Patents, P.O. 1450, Alexandria, VA 22313-1450 on June 6, 2003.

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Marilyn Bass June 6, 2003

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